JXR151T User Manual

Version: V1.1

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1 summarize

The JXR151T is a high-precision, real-time clock chip with an internal 32.768KHz DTCXO (temperature complementary crystal oscillator) with an I² C interface.

The chip has a minimum unit of seconds and can realize automatic leap year correction; it can also provide timed alarm interrupt, fixed cycle interrupt, time update interrupt output and 32.768KHz/1024Hz/1Hz clock output.

2 specifications

- Built-in high precision 32.768KHz DTCXO
- Supports high-speed I² C bus protocol (400KHz)
- Timed alarm interrupt function (settable: day of the week, day of the week, hour, minute)
- Fixed cycle interrupt function
- Time update interrupt function
- 32.768KHz/1024Hz/1Hz clock output with enable control
- Automatic leap year adjustment function
- Temperature compensation circuit operating voltage range: 2.2V~5.5V
- Clock circuit operating voltage range: 1.8V~5.5V
- Low current power consumption: 2.2μA@3V(Typ)

3 Structural Block Diagram

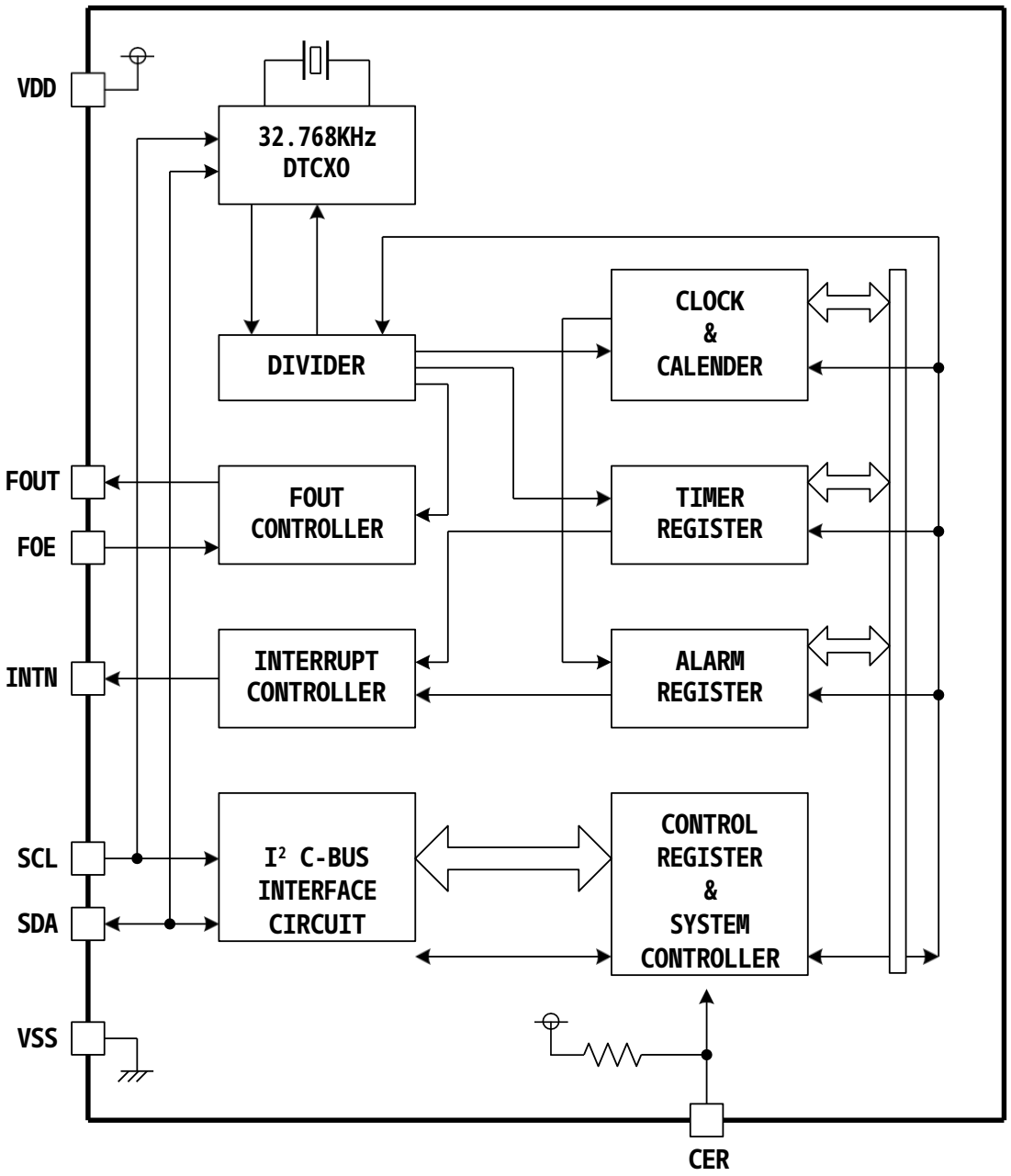


Figure 3-1 JXR151T System Block Diagram

4 Pin Definitions

4.1 Package form

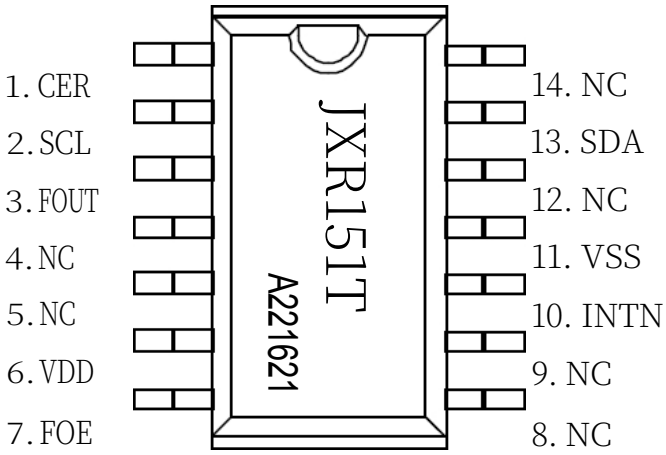


Figure 4-1 JXR151T Package Type

4.2 Pin Function

Table 4-1 JXR151T Pin Definitions

Pin name	I/O	Function
1. CER	IN	*For factory testing (no connection required, remain suspended)
2. SCL	IN	I² C Bus communication serial clock inputs
3. FOUT	OUT	32768Hz frequency output port, controlled by FOE, when FOE=1, output 32768Hz Clock; FOE=0, output is high resistance state
4/5/8/9/12/14: NC	--	No connection required, stays suspended
6. VDD	POWER	Power Positive
7. FOE	IN	FOUT Output Enable
10. INTN	OUT	Interrupt Output Port, N-ch Open Drain Outputs
11. VSS	GROUND	Power Ground
13. SDA	I/O	I2C bus communication data transfer side, N-ch open-drain outputs

5 Absolute electrical indicators

Table 5-1 Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Supply voltage*1	VDD	Voltage between VDD and VSS	-0.5 to 6	V
Input Voltage*1, *2	VIN	FOE, SCL, SDA pins	-0.5 to VDD+0.3	V
Output Voltage*1, *2	VOUT	FOUT, SDA, INTN pins	-0.5 to VDD+0.3	V
Storage temperature	TSTG	Dispersed, unpackaged	-55 to 150	°C

*1: Each electrical indicator must not exceed the maximum rating range in the above table at any time, otherwise it will cause deterioration of the relevant parameters, decrease in reliability or even chip failure.

*2: VDD here refers to the VDD range under recommended operating conditions.

6 Recommended Operating Conditions

Table 6-1 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	VDD	Interface Voltage	1.8	3.0	5.5	V
Temperature compensation voltage	VTEM	Temperature complementary circuit operating voltage	2.2	3.0	5.5	V
Clock operating voltage	VCLK	Oscillator Module Operating Voltage	1.8	3.0	5.5	V
operating temperature	TOPR	---	-40	25	85	°C

*Any operation outside the recommended range in the above table may significantly affect the reliability of the chip.

7 frequency characteristic

Table 7-1 Frequency Characteristics

Item	symbol	Condition	MIN	TYP	MAX	Unit
frequency stability	Δf/f	Ta=0° C~50° C, VDD=2.2V~5V			±3.0	$\times 10^{-6}$
		Ta=-40° C~85° C, VDD=2.2V~5V			±5.0	
voltage	Δf/f/V	Ta=25° C, VDD=2.2V~5.5V		±0.5	±1.0	$\times 10^{-6}$ /V

factor						
Starting time	TSTA	Ta=25° C, VDD=1.8V			0.9	S
		Ta=-40° C~85° C, VDD=1.8V~5.5V			2.0	
ageing	fa	Ta=25° C, VDD=3.0V, first year			±1.0	$\times 10^{-6}$ /year

8 Electrical Characteristics

8.1 DC Characteristics

Table 8-1 DC Gas Characteristics

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current power consumption	IDD1	FOE=GND FOUT=Hi-Z	VDD=5V		2.4		μA
	IDD2		VDD=3V		2.3		
Current power consumption	IDD3	FOE=VDD FOUT=32.768KHz CL=0pF	VDD=5V		3.6		μA
	IDD4		VDD=3V		2.9		
Current power consumption	IDD5	FOE=VDD FOUT=32.768KHz CL=30pF	VDD=5V		7.5		μA
	IDD6		VDD=3V		6.2		
High Input Level	VIH	cer, foe, scl. SDA pins	VDD=2.2V~5.5V	0.7*VDD		VDD	V
Low Input Level	VIL	cer, foe, scl. SDA pins	VDD=2.2V~5.5V	0		0.3*VDD	V
High output level	VOH	FOUT pin	IOH=-1mA	VDD-0.3		VDD	V
Low Output Level	VOL	FOUT, INTN pins	IOL=1mA	GND		GND+0.3	V
		SDA pin	VDD≥2V IOL=3mA	GND		GND+0.3	V
Input Leakage Current	ILK	FOE, SCL, SDA, VIN=VDD or GND		-0.3		0.3	μA
Output Leakage Current	IOZ	INTN, FOUT, SDA, VIN=VDD or GND		-0.3		0.3	μA

8.2 AC Characteristics

Table 8-2 AC Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL Clock Frequency	fSCL	---			400	KHz
Starting condition establishment time	tSU;STA	---	0.6			μS
Starting condition hold time	tHD;STA	---	0.6			μS
Data transfer setup time	tSU;DAT	---	100			nS
Data Transfer Hold Time	tHD;DAT	---	0		700	nS
Termination condition establishment time	tSU;STO	---	0.6			μS
Bus Idle Time	tBUF	Between the termination condition and the start condition	1.3			μS
SCL Low Level Time	tLOW	---	1			μS
SCL high level time	tHIGH	---	1			μS
SCL, SDA Rise Time	tr	---			0.3	μS
SCL, SDA downtime	tf	---			0.3	μS
Bus Burr Duration	tSP	---			50	nS
FOUT Output Duty Cycle	Duty	Calculated with output at 50% of V_{DD}	40	50	60	%

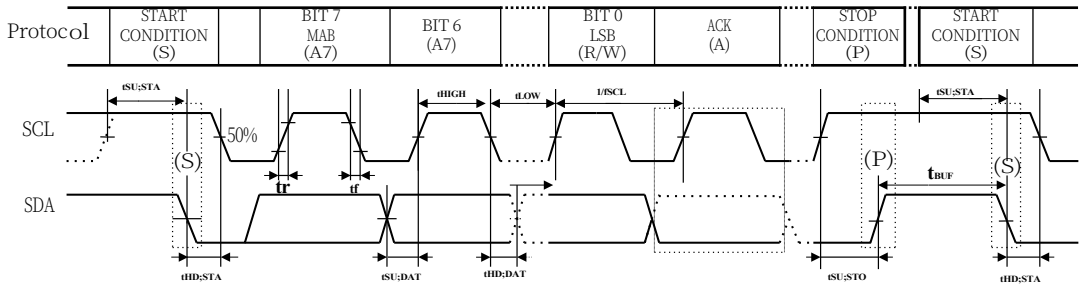


Figure 8-1 I²C Timing Legend

*I²C data transfer is located between the start condition and the termination condition, the data transfer operation must be completed within 0.95S time, after which the I²C bus will be reset by the internal timer.

9 processor register

9.1 Register Summary Table

Table 9-1 Register List

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	SEC	character used in Taiwan as a substitute for a real name (like "X" in English)	40	20	10	8	4	2	1
1	MIN	character used in Taiwan as a substitute for a real name (like "X" in English)	40	20	10	8	4	2	1
2	HOUR	character used in Taiwan as a substitute for a real name (like "X" in English)	character used in Taiwan as a substitute for a real name (like "X" in English)	20	10	8	4	2	1
3	WEEK	character used in Taiwan as a substitute for a real name (like "X" in English)	6	5	4	3	2	1	0
4	DAY	character used in Taiwan as a substitute for a real name (like "X" in English)	character used in Taiwan as a substitute for a real name (like "X" in English)	20	10	8	4	2	1
5	MONTH	character used in Taiwan as a substitute for a real name (like "X" in English)	character used in Taiwan as a substitute for a real name (like "X" in English)	character used in Taiwan as a substitute for a real name (like "X" in English)	10	8	4	2	1
6	YEAR	80	40	20	10	8	4	2	1
7	RAM	●	●	●	●	●	●	●	●

8	MIN Alarm	AE	40	20	10	8	4	2	1
9	HOUR Alarm	AE	●	20	10	8	4	2	1
A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		●	20	10	8	4	2	1
B	Timer Counter 0	128	64	32	16	8	4	2	1
C	Timer Counter 1	●	●	●	●	2048	1024	512	256
D	Extension Register	character used in Taiwan as a substitute for a real name (like "X" in English)	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
E	Flag Register	character used in Taiwan as a substitute for a real name (like "X" in English)	character used in Taiwan as a substitute for a real name (like "X" in English)	UF	TF	AF	character used in Taiwan as a substitute for a real name (like "X" in English)	VLF	VDET
F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	character used in Taiwan as a substitute for a real name (like "X" in English)	character used in Taiwan as a substitute for a real name (like "X" in English)	RESET

* Make sure that you write legal values to the calendar and clock registers, otherwise the chip will not be able to perform correct timing operations.

*The register bits marked with ○ are read-only bits with a read value of "0", while the register bits marked with ● can be used as RAM to perform read and write operations.

*If the alarm interrupt function is not set (AIE="0") registers 8~A can be used as RAM.

*If the fixed-cycle interrupt function is not set (TE=TIE="0") registers B and C can be used as RAM.

The *UF, TF, AF, VLF and VDET bits are only allowed to be written to "0".

* CSEL0 bit is preset to "1" when the chip is powered up, FSEL1, FSEL0, CSEL1, VLF, UIE, TIE, AIE

The bit is preset to "0".

9.2 Register Details

9.2.1 Clock and Calendar Registers (Registers 0~6)

- data format

  Except for the day register (register 3), the data is in BCD code format. For example, the value of the seconds register is "0101 1001".

This means that the current time is 59 seconds.

The timekeeping is fixed at 24 hours.

- Annual registers and leap years

The time range of the year register is from 00 to 99, after 99, it returns to 00; when the value represented by the year register can be divided by 4, the year is recognized as a leap year; the validity period of the calendar is from 2000 to 2099.

- Day of the week register

  The day of the week register has 7 valid bits (bit0~bit6) each valid bit represents a day from Monday to Sunday.

Therefore, only one bit of this register is allowed to be "1".

Table 9-2 Weekly Register Correspondence Table

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	last week
0	0	0	0	0	0	1	date
0	0	0	0	0	1	0	-
0	0	0	0	1	0	0	stupid (Beijing dialect)
0	0	0	1	0	0	0	surname San
0	0	1	0	0	0	0	4
0	1	0	0	0	0	0	5
1	0	0	0	0	0	0	6

9.2.2 Alarm Register (Register 8~A)

Alarms can be set for X hours and X minutes on X days of the week or X hours and X minutes on X days of the month (Weekly Alarm Mode and Daily Alarm Mode) and the alarm mode can be set with the WADA bit in Register D.

Each alarm register has an AE (Alarm Enable) bit (bit7) When the AE bit of an alarm register is "0", the set value of the register should be compared with the corresponding timing register, and an alarm interrupt will be output when the value is the same; if the AE bit is "1", the corresponding alarm register value will be ignored, i.e., there is no need to compare the corresponding alarm register with the timing register, and it is always considered that the alarm register value is the same as the corresponding timing register value. If the AE bit is "1", the corresponding alarm register value will be ignored, i.e., there is no need to compare the corresponding alarm register with the timing register, and the alarm register value is always considered to be the same as the corresponding timing register value.

When the week alarm mode is selected, the days of the week can be selected at the same time, i.e., WEEK ALARM in register A

Function bit0~bit6 can have several bits as "1" at the same time. Refer to Table 9-3 for

the corresponding relationship in weekly alarm mode.

Table 9-3 Weekly Alarm Mode Register A Correspondence Table

register	Function	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A	Weekly Alarm	6	5	4	surname San	stupid (Beijing dialect)	-	date

9.2.3 Fixed Cycle Counter Control Register (Register B, C)

These two registers are used to set the preset countdown value for fixed cycle interrupt. When the value in the above two registers changes from 001h to 000h, a fixed cycle interrupt event occurs, TF is set to "1" and a low level is output on INTN (if TIE is "1"); after that, the B and C registers are reset to the preset value and the countdown process starts again. TF is set to "1" and INTN outputs a low level (if TIE is "1"); after that, B and C registers are reset to the preset values and the countdown process starts again.

9.2.4 Control Registers and Flag Registers (Registers D~F)

- WADA bit

  Alarm interrupt mode selection bit, when set to "1", for the day alarm mode, when set to "0", for the week alarm mode.
- USEL bit

  Used to set the period of the time update interrupt; this bit is an indeterminate value when the chip is powered on, and needs to be configured manually during use.

Table 9-4 Time Update Interrupt Mode Selection

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- TE bit

  When this position is set to "1", the fixed-cycle interrupt counter starts counting down, and when it is set to "0", it stops counting down.
- FSEL bit

  It is used to set the output frequency of FOUT port, and refer to Table 9-5 for the specific configuration; the default value is "00" after the chip is powered on.

Table 9-5 FOUT Output Frequency Selection

FSEL1	FSEL0	FOUT frequency
0	0	32.768KHz *Default
0	1	1024Hz
1	0	1Hz
1	1	32.768KHz

- TSEL bit

  Used to set the count period for fixed-cycle interrupts.

Table 9-6 Fixed-Cycle Interrupt Count Period Selection

TSEL1	TSEL0	Source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

- AF, TF, UF Bit

  The flag bits for alarm interrupt, fixed cycle interrupt, and time update interrupt,

respectively; when the above interrupt events occur, the corresponding flag bit is set to "1". When the above interrupt events occur, the corresponding flag bit will be set to "1". The flag bit will be maintained as "1" until it is cleared to "0" manually, and it is prohibited to manually set the above flag bit to "1".

• AIE, TIE, UIE Bit

It is used to set the interrupt signal output on INTN pin when alarm interrupt, fixed cycle interrupt and time update interrupt events occur respectively; the default value of the three bits is "0".

The interrupt signal output on the INTN pin is the logical or of the alarm interrupt, fixed cycle interrupt, and time update interrupt, and the interrupt flag bit is used to determine the specific interrupt situation and determine the interrupt signal output.

• VLF Bit

Low Voltage Detection Flag Bit; this bit is set to "1" when the clock circuit fails to operate normally due to the detection of the power supply voltage dropping below 1.8V, or when the power-on reset signal is detected. This flag bit will be maintained as "1" until it is cleared to "0" manually, and it is prohibited to set this flag bit to "1" manually.

• VDET Bit

Voltage Detection Flag Bit; this bit is set to "1" when the power supply voltage is detected to drop below 2.2V, causing the temperature compensation circuit to be unable to operate normally. This flag bit will remain at "1" until it is cleared to "0" manually, and it is prohibited to manually set this flag bit to "1".

• CSEL Bit

Used to set the time interval for the temperature compensation circuit to start; the default value is "01" (2S) after the chip is powered on.

Table 9-7 Selection of warm-up interval

CSEL1	CSEL0	Operation interval
0	0	0.5S
0	1	2S *Default
1	0	10S
1	1	30S

• RESET Bit

When RESET is set to "1", the registers under seconds are reset and the clock is stopped; the temperature compensation and VLF/VDET voltage detection functions are disabled.

The RESET bit, which is set to "1", clears to "0" again in the following three cases: when an I² C termination condition is detected, when a restart condition is detected, or when the I² C bus reset occurs after 0.95 S. The VLF/VDET flag bit clears to "0" at the same time, resetting the power supply voltage detection function. At the same time, the VLF/VDET flag bit clears to "0", resetting the supply voltage detection function.

10 interrupt function

10.1 Alarm interruption

Alarm interruptions can generate alarm interrupt events on set days of the week, days of the week, hours, and minutes.

10.1.1 Alarm interrupt timing

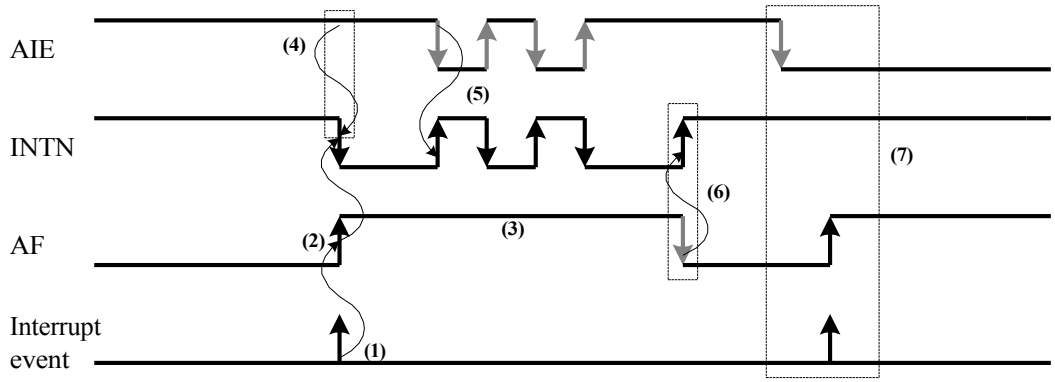


Figure 10-1 Alarm Interrupt Timing

(1) Set the hour, minute, date or day of the week information corresponding to the alarm interruption and the WADA register to generate an alarm interruption event when the set time matches the current time.

(2) The AF flag bit is set to "1" when an alarm interrupt event is generated.

(3) The AF register will remain at "1" until it is manually cleared to "0".

(4) When an alarm interrupt event occurs, if AIE="1", INTN outputs low level; if AIE="0", INTN remains Hi-Z.
Status.

(5) If the AIE is set to "0" during the INTN="0" period, INTN immediately returns to the Hi-Z state; if an alarm interrupt event occurs and AF
AIE can be used to control the output state of INTN before the register is cleared to "0".

(6) Clearing the AF register to "0" clears the alarm interrupt output, and INTN changes from "0" to Hi-Z status immediately.

(7) If AIE="0" when an alarm interrupt event occurs, INTN maintains the Hi-Z state and does not output a low level.

10.1.2 Alarm Interrupt Related Registers

Table 10-1 Alarm Interrupt Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8	MIN Alarm	**AE**	40	20	10	8	4	2	1
9	HOUR Alarm	**AE**	●	20	10	8	4	2	1
A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		●	20	10	8	4	2	1
D	Extension Register	character used in Taiwan as a substitute for a real name (like "X" in English)	**WADA**	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
E	Flag Register	character used in Taiwan as a substitute for a real name (like "X" in English)	character used in Taiwan as a substitute for a real name (like "X" in English)	UF	TF	**AF**	character used in Taiwan as a substitute for a real name (like "X" in English)	VLF	VDET
F	Control Register	CSEL1	CSEL0	UIE	TIE	**AIE**	character used in Taiwan as a substitute for a real name (like "X" in English)	character used in Taiwan as a substitute for a real name (like "X" in English)	RESET

- When configuring the Alarm Interrupt Register, it is recommended that the AIE be set to "0" first to prevent unnecessary hardware interrupts from being generated during operation.
- WADA is used to select the alarm mode, when set to "1", it is the daily alarm mode, when set to "0", it is the weekly alarm mode.
- The occurrence of an alarm interrupt event sets the AF flag position "1", which will remain "1" until it is manually set to "0".
- When an alarm interrupt event occurs, the AIE determines whether to generate an interrupt signal output (AIE="1", then INTN="0"; AIE="0", then INTN= Hi-Z)
- An AE bit of "0" indicates that the corresponding register needs to be compared with the clock or calendar register; if the AE bit is "1", the corresponding register is not compared, i.e., it is assumed that the register always matches the corresponding clock or calendar register. Refer to the following example:
  (1) When register A is set to "80", only the minute and hour alarm registers need to be compared to the corresponding clock registers, ignoring the day/date registers; therefore, an alarm interrupt event will be generated every day as

long as the hour and minute registers match.

(2) Setting the AE bits in the 8, 9, and A registers to "1" causes an alarm interrupt event to be generated once per minute.

10.2 Fixed-cycle interruptions

Fixed-cycle interrupts can generate interrupt alarm events at a fixed cycle between 244.14μS and 4095min.

10.2.1 Fixed-cycle interrupt timing

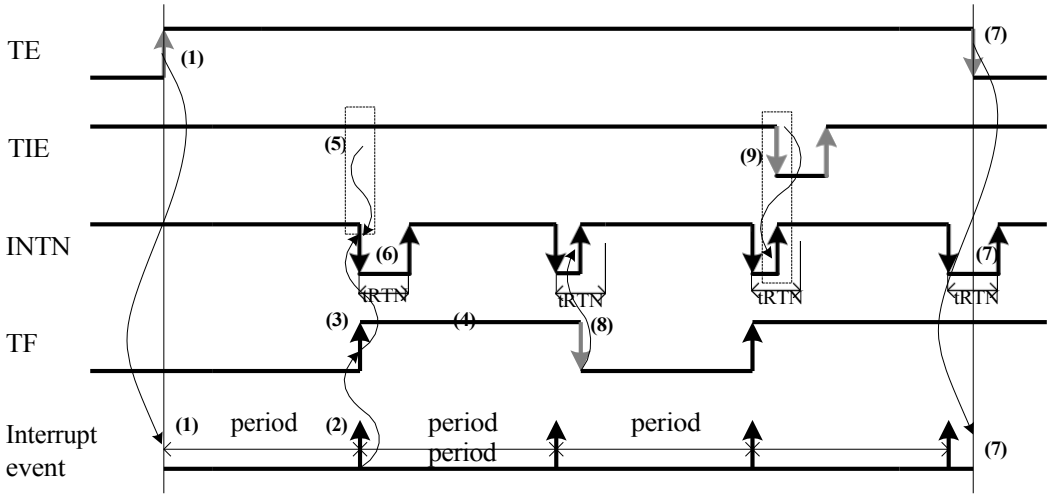


Figure 10-2 Fixed-Cycle Interrupt Timing

(1) When "1" is written to the TE bit, the fixed cycle counter starts counting down from the preset value.

(2) An interrupt event is generated when the fixed-cycle counter counts from 001h to 000h; the counter resets to the preset value and continues to the next count.

(3) The TF register is set to "1" when a fixed-cycle interrupt event occurs.

(4) The TF register will remain at "1" until it is manually cleared to "0".

(5) When a fixed-cycle interrupt event occurs, if TIE="1", INTN outputs low; if TIE="0", INTN remains in Hi-Z state.

(6) The INTN output goes low for tRTN, after which the Hi-Z state is automatically restored until the next interrupt signal is output.

(7) When "0" is written to the TE bit, the fixed-cycle counter stops counting, and Hi-Z is output from INTN (if "0" is written to the TE bit in the (During INTN="0", INTN resumes Hi-Z state after tRTN time)

(8) If TF is cleared to "0" during INTN="0", INTN immediately returns to the Hi-Z state.

(9) When the TIE is written to "0", the INTN restores the Hi-Z state immediately. If the TIE is written to 1 again during the tRTN period, the INTN will return to the Hi-Z state immediately.
It will still be in Hi-Z condition.

10.2.2 Fixed-cycle interrupt-related registers

Table 10-2 Fixed-Cycle Interrupt Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B	Timer Counter 0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
C	Timer Counter 1	●	●	●	●	**2048**	**1024**	**512**	**256**
D	Extension Register	character used in Taiwan as a substitute for a real name (like "X" in English)	WADA	USEL	**TE**	FSEL1	FSEL0	**TSEL1**	**TSEL0**
E	Flag Register	character used in Taiwan as a substitute for a real name (like "X" in English)	character used in Taiwan as a substitute for a real name (like "X" in English)	UF	**TF**	AF	character used in Taiwan as a substitute for a real name (like "X" in English)	VLF	VDET
F	Control Register	CSEL1	CSEL0	UIE	**TIE**	AIE	character used in Taiwan as a substitute for a real name (like "X" in English)	character used in Taiwan as a substitute for a real name (like "X" in English)	RESET

- When configuring the fixed-cycle interrupt registers, it is recommended that TE and TIE be set to "0" first to prevent unnecessary hardware interrupts from being generated during operation.
- TSEL1 and TSEL0 are used to set the countdown period for fixed-cycle interrupts, and the automatic reset time of the interrupt signal on the INTN pin is related to the countdown period.

Table 10-3 Fixed-Cycle Interrupt Counting Periods and Auto Reset Times

TSEL1	TSEL0	Source clock	Auto reset time
0	0	4096Hz	0.122mS
0	1	64Hz	7.8125mS
1	0	1Hz	7.8125mS
1	1	1/60Hz	7.8125mS

- Registers B and C set the default value of the counter (001h~FFFh) When the counter counts down to 000h with the counting period set by TSEL, a fixed-cycle interrupt event is generated.
- TE is the enable control bit of fixed cycle counter, when TE="1", the counter starts counting down; when TE="0", the counter stops counting and terminates the fixed cycle interrupt function.

- The occurrence of a fixed-cycle interrupt event sets the TF flag position "1", which will remain "1" until it is manually set to "0".
- When a fixed-cycle interrupt event occurs, TIE determines whether to generate an interrupt signal output (TIE="1", then INTN="0"; TIE="0", then INTN=Hi-Z)

Table 10-4 Fixed-Cycle Interrupt Cycle Examples

Timer counter set value	Source clock			
	4096Hz	64Hz	1Hz	1/60Hz
0	---	---	---	---
1	244.14μS	15.625mS	1S	1min
……	……	……	……	……
2048	500mS	32S	2048S	2048min
……	……	……	……	……
4095	0.9998S	63.984S	4095S	4095min

10.3 Interrupted time updates

Depending on the set value, the time update interrupt generates an interrupt alarm event with a second update or a minute update.

10.3.1 Time Update Interrupt Timing

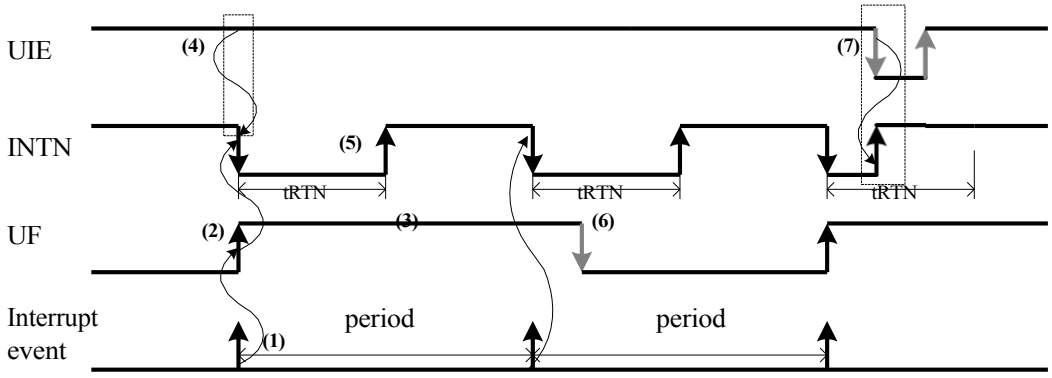


Figure 10-3 Time Update Interrupt Timing

(1) The USEL register determines whether the chip is in the second update interrupt or minute update interrupt state, and generates a time update interrupt event when the corresponding second register or minute register is updated.

(2) The UF register is set to "1" when the time update interrupt event is generated.

(3) The UF register will remain at "1" until it is manually cleared to "0".

(4) When the time update interrupt event occurs, if UIE="1", INTN outputs low level; if UIE="0", INTN remains as
Hi-Z status.

(5) The INTN output goes low for tRTN, after which the Hi-Z state is automatically restored until the next interrupt signal is output.

(6) If UF is cleared to "0" during INTN="0", INTN will return to Hi-Z state after tRTN time.

(7) If UIE is set to "0" during the INTN="0" period,INTN immediately returns to theHi-Z state and the interrupt signal output ends. If UIE is set to "0" during tRTN="0", INTN immediately resumes Hi-Z state and the interrupt signal output ends.
Write the UIE to 1 again during this period and the INTN will remain Hi-Z.

10.3.2 Time Update Interrupt Related Registers

Table 10-5 Time Update Interrupt Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
D	Extension Register	character used in Taiwan as a substitute for a real name (like "X" in English)	WADA	**USEL**	TE	FSEL1	FSEL0	TSEL1	TSEL0
E	Flag Register	character used in Taiwan as a substitute for a real name (like "X" in English)	character used in Taiwan as a substitute for a real name (like "X" in English)	**UF**	TF	AF	character used in Taiwan as a substitute for a real name (like "X" in English)	VLF	VDET
F	Control Register	CSEL1	CSEL0	**UIE**	TIE	AIE	character used in Taiwan as a substitute for a real name (like "X" in English)	character used in Taiwan as a substitute for a real name (like "X" in English)	RESET

- When configuring the time update interrupt register, it is recommended that the UIE be set to "0" first to prevent unnecessary hardware interrupts from being generated during operation.
- The USEL signal is used to set the interrupt mode to second update or minute update.

Table 10-6 Time Update Interrupt Modes

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- The occurrence of a time update interrupt event sets the UF flag position "1", which will remain "1" until it is manually cleared to "0".
- When a time update interrupt event occurs, the UIE determines whether to generate an interrupt signal output (UIE="1", then INTN="0"; UIE="0", then INTN=Hi-Z)

11 I C² Bus Interface

11.1 I C² Bus Features

I² C is a bi-directional communication interface, its signal line SDA and clock line SCL should be connected to VDD through pull-up resistors; the ports connected to the I² C bus must be open-drain structure in order to realize multi-device line and connection.

11.2 data transmission

1bit of data can be transmitted per SCL clock cycle. When sending data, the data on the SDA line changes during SCL low; when receiving data, stable and valid data can be obtained from the data line SDA during SCL high.

11.3 Starting and ending conditions

During the idle state, SCL and SDA are held high. the falling edge of SDA during SCL high is used as the start condition for I² C communication; the rising edge of SDA during SCL high is used as the termination condition for I² C communication.

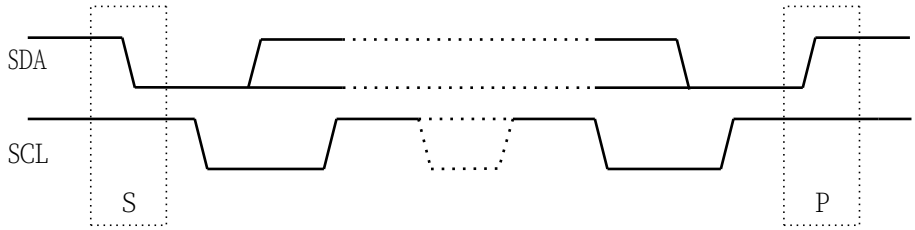


Figure 11-1 I² C Starting Conditions and Ending Conditions

11.4 Device selection (from address)

I² C bus devices do not have a chip select signal. The master device selects the corresponding slave device by sending a unique fixed device number (slave address), and the selected slave device sends an answer signal to establish communication with the master device.

The slave address consists of 7 bits of data, 4 bits (Group 1) + 3 bits (Group 2), and the slave address of the JXR151T is "0110010". The slave address of the JXR151T is "0110010". During communication, the slave address and the R/W selection bit are sent in the form of 8bit data.

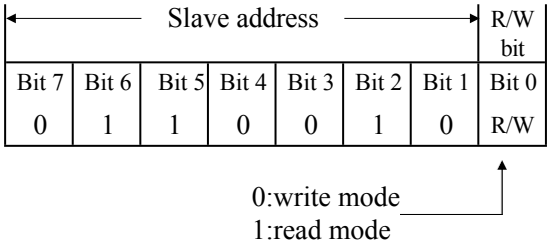


Figure 11-2 I² C Slave Address Schematic

11.5 System Configuration

The device that controls the data transmission is called the "master device", and the devices that are controlled by the master device are called "slave devices"; the device that sends the data is called the "sender", and the device that receives the data is called the "receiver". The device that sends data is called the "sender" and the device that receives data is called the "receiver".

In the JXR151T system, the CPU or other control device is the master device, and the JXR151T chip itself is the slave device; both master and slave devices can be used as the transmitter or receiver.

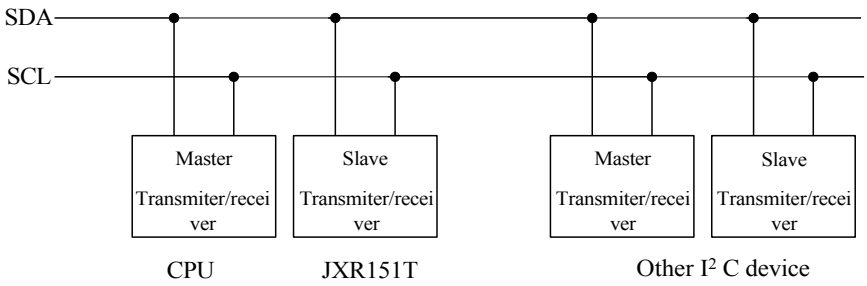


Figure 11-3 I² C System Configuration

11.6 response signal

I² The C bus has no limit on the number of bytes that can be transferred between the start and end conditions. After each byte of data has been transferred, the transmitter releases the SDA bus and provides 1 SCL clock to receive the answer signal. If the receiving side successfully receives 8bit data, it must set SDA to "0" after the end of the clock of transmitting the last 1bit data, and the transmitting side will use this low level as the answer signal for successful data transmission; after 1 clock cycle, the receiving side releases SDA bus and is ready to receive new data.

I² C The bus terminates data transfer when the following conditions are met:

(1) When the master device acts as a transmitter, it sends a termination condition after receiving an answer signal from the slave device.

(2) When the master device acts as the receiver, it sends a "1" as an answer signal after successfully receiving 8-bit data, and then sends the termination condition.

11.7 I C² Bus Control

This subsection describes the I² C bus communication timing for the case where the CPU acts as the master device and the JXR151T acts as the slave device.

11.7.1 Designated Address Write Operation

JXR151T has an address auto-increment function. After setting the operation address, you only need to send data continuously, and the address bits can be incremented automatically.

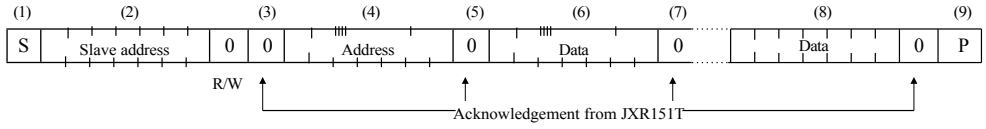


Figure 11-4 Designated Address Write Operation

(1) CPU sends start condition [S].

(2) The CPU sends the JXR151T slave address and sets it to write mode with the R/W bit.

(3) The JXR151T generates an answer signal.

(4) The CPU sends the write register address to the JXR151T.

(5) The JXR151T generates an answer signal.

(6) The CPU sends data to the register corresponding to the address specified in (4).

(7) The JXR151T generates an answer signal.

(8) Repeat the process of (6) (7) and the address of the write register in the JXR151T is automatically incremented.

(9) CPU sends termination condition [P].

11.7.2 Designated address read operation

After writing to the register, the CPU can read the register data by setting the read mode.

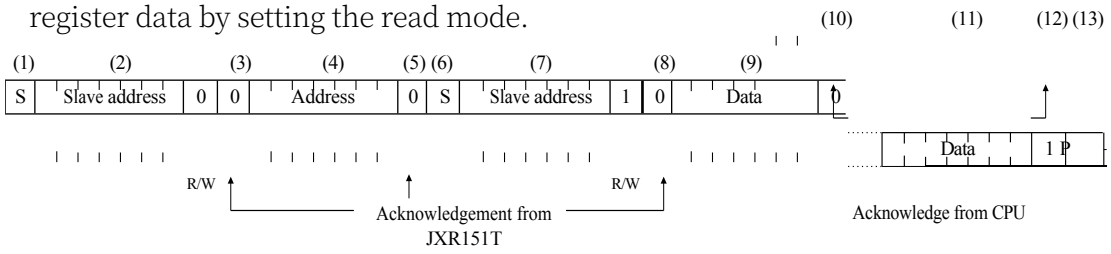


Figure 11-5 Designated Address Read Operation

(1) CPU sends start condition [S].

(2) The CPU sends the JXR151T slave address and sets it to write mode with the R/W bit.

(3) The JXR151T generates an answer signal.

(4) The CPU sends the read register address to the JXR151T.

(5) The JXR151T generates an answer signal.

(6) The CPU resends the start condition.

(7) The CPU sends the JXR151T slave address and sets it to read mode with the R/W bit.

(8) The JXR151T generates an answer signal; after that, the CPU acts as the receiver and the JXR151T acts as the transmitter.

(9) The JXR151T transmits the data in the register corresponding to the address specified in (4).

(10) The CPU sends an answer signal to the JXR151T.

(11) Repeat the procedure (9) (10) and the address of the read register in the JXR151T will be incremented automatically.

(12) The CPU sends an answer signal to the JXR151T.

(13) CPU sends termination condition [P].

11.7.3 Unassigned address read operation

The master device can read the contents of all registers in the slave device by entering the read mode directly. If the operation is preceded by a read operation, the read operation is continued from the address of the register that has been read + 1. If the operation is preceded by a write operation, the read operation is started from the first register address corresponding to the write operation.

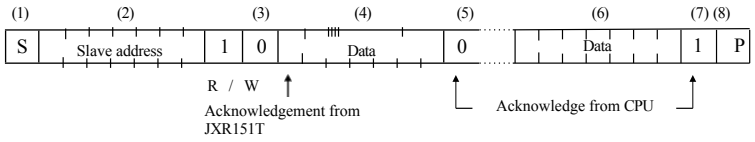


Figure 11-6 Unspecified Address Read Operation

(1) CPU sends start condition [S].

(2) The CPU sends the JXR151T slave address and sets it to read mode with the R/W bit.

(3) The JXR151T generates an answer signal; after that, the CPU acts as the receiver and the JXR151T acts as the transmitter.

(4) The JXR151T automatically increments the register address and sends the register data.

(5) The CPU sends an answer signal to the JXR151T.

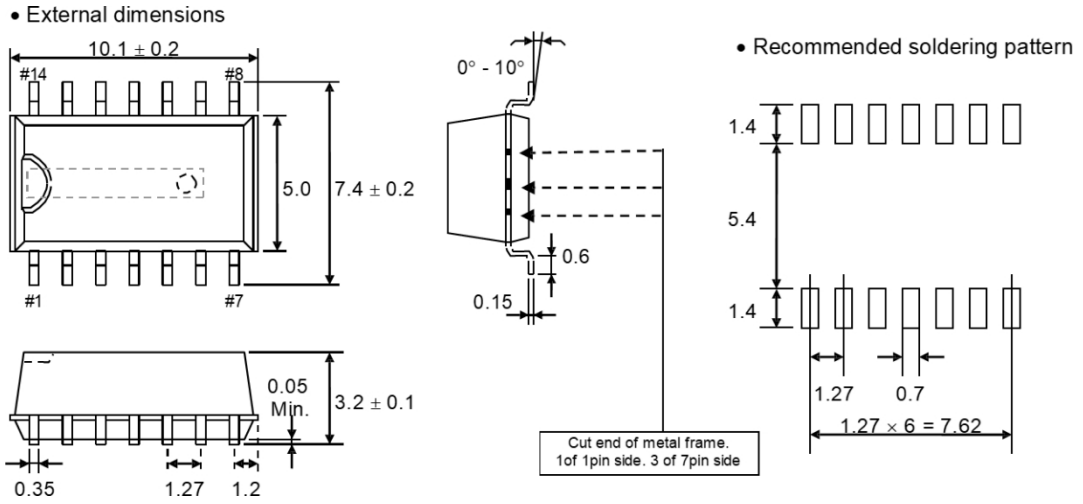
(6) Repeat the process of (4) (5) and the address of the read register in the JXR151T will be incremented automatically.

(7) The CPU sends an answer signal to the JXR151T.

(8) CPU sends termination condition [P].

appendice

Package Size

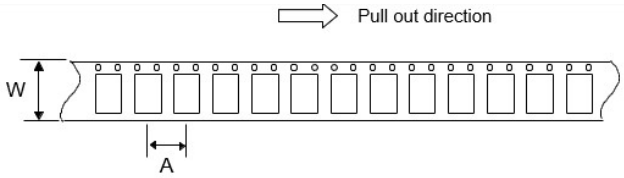


Packaging specification

SOP Emboss Taping (TE2)

Symbol	SOP14
A	8
W	16

Unit : mm



Symbol	SOP14
A	330
W	16.4
Contents	1000 pcs

Unit : mm